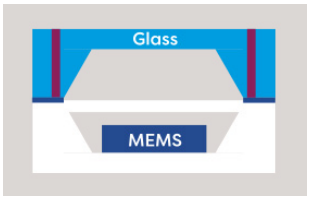
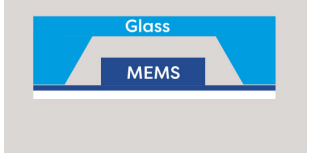
Wafer level packaging for MEMS

Hermetically sealed and reliable packaging solutions based on glass-Si materials for System-in-package (SiP) and MEMS applications

Creating a hermetically sealed workspace in which "the heart" of the application can operate under ideal technological conditions, is an ongoing challenge. For example, while some cases need a high vacuum inside the workspace, others might require a specific gas combination.



TGV module (through glass metallised vias)



WLC module (wafer level glass capping)

Packaging on wafer level

Particularly for MEMS applications there is an increased risk of damages if and when unpackaged dies are handled by standard 'pick-and-place' processes. Therefore, it is crucial to cover the chips with a robust mechanical package before any dicing and assembling processes start. Whatever the final design of an application – the generic solution to this particular issue is a 'capping wafer', based on glass or silicon, or even a combination of materials.

When necessary more functionalities can be integrated into the package, as the described example of the Energy Harvester from microGen Systems, Inc. (USA) shows hereinafter.

MEMS Energy Harvester

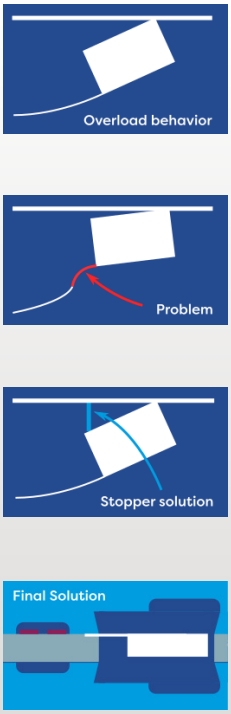
An 'energy harvester' is a small size nano-generator device, generating minor amounts of electrical energy, such as mechanical movement, from environmental sources. microGen's Energy Harvester converts external vibrations - a cantilever is triggered to mechanical oscillation – into electrical energy by using the piezoelectric effect.

*"**Our product solution required a package with integrated overload protection.**"* Kathleen Vaeth, VP of Engineering, microGen.

Project example

Kathleen Vaeth, VP of Engineering at microGen Systems Inc., explains: "The objective of this project with Micronit was to create a package for a silicon based energy harvesting device. Important constraint: the solution must provide an integrated overload protection."

microGen Systems Inc. Energy Harvesters packaged with Micronit's unique glass capping wafers



The WLC result - cross section view of the multilayer cavity feature

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The development result is an "impact stopper structure" that is based on the dual-depth cavity principle, composed of two bonded glass wafers. The silicon sensor wafer is encapsulated in two symmetric glass capping wafers. The dual-depth cavities provide enough room for vibration, while the open cavities above the bond pads enable subsequent access for electronic interconnections.

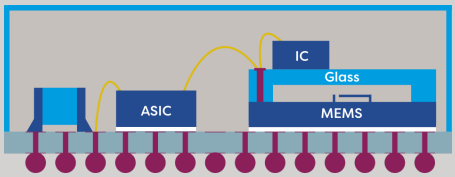
The mainly applied technologies in this project are wet etching, laser machining and wafer bonding on 200 mm glass wafer size.

"The new wafer level capping solution improved our cost efficiency, increased the component's robustness by factor 5 and helped us to achieve a unique product positioning resulting in a significant sales increase." Michael Perrotta, CEO, microGen.

Trends in Electronics: System-in-Package (SiP)

Trends in 'Wafer-Level-Packaging' are also forced by general development directions in electronics: Semiconductor solutions are supposed to keep decreasing in size and become more functional at the same time. In addition, the number of applications with small to middle size volume manufacturing is rapidly growing.

Aiming to achieve the markets need for further miniaturisation through higher integration on wafer space, faces limits set by physics. Therefore, chip manufacturers follow differentiated paths in order to better utilise an available installation space. With this in mind – and tailor made for the specific application - several specialised chips (e.g. GPS, RF, NFC but also MEMS components like gyroscopes or mirrors) can configure and integrate better into one system (2D on the surface or 3D in space) as opposed to a single chip system. In this case, a uniformed chip, that functions as a System-on-Chip (SoC) for many different applications is no longer up for consideration, but the application itself is. Moreover, the requirements for smartphones are different from those for medicine. So, the solution won't easily be found in System-on-Chip (SoC), but increasingly in the System-in-Package (SiP) approach associated with an increased utilisation of 'Wafer-level-packaging'.



WLC: Wafer level capping (glass lid) in a SiP- application

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